An Antenna Diversity MMIC Vector Modulator for HIPERLAN with Low Power Consumption and Calibration Capability

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***Abstract*—The design and performance of a vector-modulator-based phase shifter for high-performance radio local area networks at 5.2 GHz is presented in this paper. Low power consumption is achieved using a 0.6-μm GaAs MESFET process. At a voltage supply of 1.4 V and with a current consumption between 3.5–7 mA, the gain is 0.6 dB and the 1-dB input compression point is -9 dBm. A full 360° phase control range is achieved by combining two of the three vectors, which have phase offsets of 120°, with variable amplitude. Chip size is only 1.3 mm^2. The proposed vector modulator applies a new circuit configuration of variable-gain amplifiers to compensate their transmission phase errors. Within a gain control range of 20 dB, the phase error can be reduced to ± 3°, which is about a factor of eight better than the results obtained by single FET amplifiers. A simple calibration procedure for the proposed vector modulators is presented to improve the manufacturing yield and to decrease the impact due to temperature changes and aging. A maximum gain error of ± 0.8 dB and a maximum phase error of ± 7° has been measured after applying this calibration to the designed vector modulator.**

***Index Terms*—GaAs, HIPERLAN, MESFETs, MMIC, phase shifter, smart antennas, vector modulator.**

I. Introduction

IT IS WELL known that adaptive antenna arrays can effectively reduce intersymbol interference in receivers for wireless local area networks (LANs). The high-performance radio local area network (HIPERLAN) plays a growing role in wireless LAN systems [1]. It has an allocated frequency band from 5.15 to 5.3 GHz with a signal bandwidth of 23.5 MHz per channel. To compete with an alternative concept using a baseband signal equalizer, low power consumption and low costs are postulated for adaptive antenna receivers. With the rapid development of monolithic microwave integrated circuits (MMIC) on semi-insulating GaAs, there is now the possibility to significantly reduce the size and costs of such receivers.

Fig. 1 shows a typical architecture of an adaptive antenna receiver. Different active antenna paths are combined after being adjusted in amplitude and phase. Single-pole double-throw (SPDT) switches can be used to switch between the antenna input signal and a calibration signal. Passive attenuators or variable-gain low-noise amplifiers [2], which are well suited for MMIC integration, are used to set the required signal amplitude. Phase shifters are needed to control the phases of the signals.

In the past, a variety of different techniques for phase shifting has been reported. Switched high-pass(HP)/low-pass (LP) phase shifters [3], reflective-type phase shifters [4], and vector modulators [5] are among the most important techniques used. Especially for high phase resolutions, switched HP/LP phase shifters require a lot of space and are not suitable for low-cost designs. Reflective-type phase shifters, which mainly consist of a 90°-hybrid and varactor diodes, are also not well suited for MMIC integration. The reason is that the quality factors and capacitance control ranges of varactor diodes of most foundry processes are relatively bad, resulting in high losses and limited phase control ranges.

Vector modulators can cover a phase shift of 360°, are able to provide gain and are well suited for MMIC integration. Signal paths with defined phase offsets (usually 90°) are weighted and combined to obtain the desired phases. Variable-gain amplifiers are required to control the amplitude of those paths. The gain should be a linear function of voltage and the phase deviation across the assumed gain range should preferably be equal to zero. The amplitude of the amplifiers can be set by analog control voltages. Usually, those voltages are read from a lookup table.

Due to variation of transit frequencies, threshold voltages, and temperature changes of the environment, the variable-gain amplifiers can have significant gain and phase deviations when using a nominal lookup table. This causes unacceptable amplitude and phase errors for the resulting output vector of vector modulators. A selection of circuits with nominal characteristics has to be made or an individual lookup table for each circuit has to be created to obtain satisfying resolutions, resulting in low production yields and high costs.

A calibration can be used to reach a high yield within process and temperature variations. However, such calibration procedures are relatively complex because the amplitude in variable-gain amplifiers cannot be controlled without influencing the phase [6].

This paper proposes a method to reduce the phase error in variable-gain amplifiers to enable a simple calibration procedure for vector modulators. Due to the small phase errors of the proposed variable-gain amplifiers, the resulting output phases and amplitudes of the vector modulator can be conveniently calculated by vector addition. The resulting phase and amplitude errors of this calibration were investigated for the designed vector modulator.

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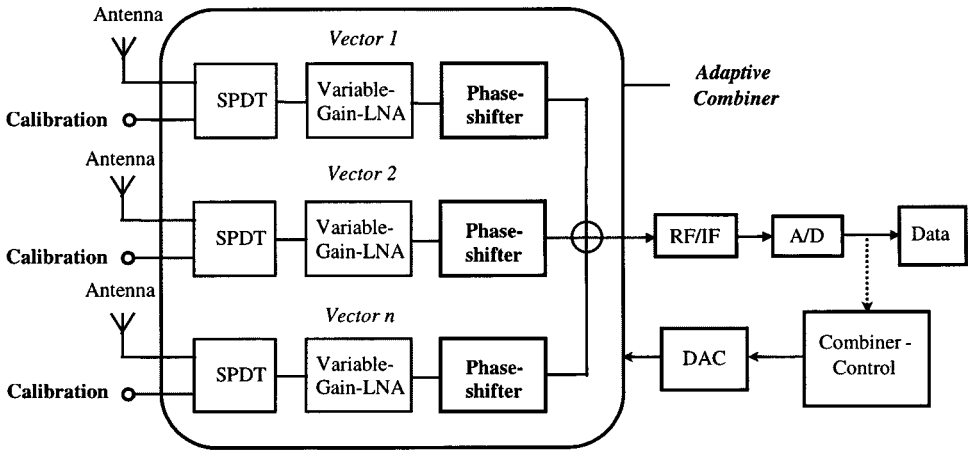

Fig. 1. Adaptive antenna receiver.

II. Transmission Phase Characteristics in Variable-Gain MESFET Amplifiers

Variable-gain amplifiers are required to control the amplitude of the different phase paths of a vector modulator. Dual- and single-gate MESFETs can be used for this purpose. Modial *et al.* [6] showed that the phase error in dual-gate MESFETs is higher than in single-gate MESFETs. Our simulations indicate the same results; thus, we use single-gate MESFETs for the variable-gain amplifiers. Simulations are performed with HP Libra using a modified TOM II large-signal model [7] for a Triquint TQTRx enhancement MESFET (E-FET). With respect to the original TOM II model, this model shows significant improvements, especially in the resistive region.

A typical variable-gain amplifier with a single MESFET in a common source configuration is shown in Fig. 2. The gain can be reduced by decreasing the gate–source voltage $(V_{\rm gs})$ or the drain voltage (V_d). The operation frequency (f) is 5.2 GHz. An E-FET with a gatewidth of 150 μm and a gate length of 0.6 μm is used, the nominal threshold voltage of the FET is 0.14 V. Input and output are reactively matched to 50 Ω. The circuit is biased by a resistor at the gate and an inductance at the drain.

A. Varying the Gate–Source Voltage with Fixed Drain–Source Voltage (Amplifier A)

Fig. 3 shows the simulated phase and amplitude characteristic of the variable-gain amplifier when the gate–source voltage is varied and the drain voltage is fixed. Within a control voltage from 0 to 0.5 V and a corresponding amplitude control range of 20 dB, a phase deviation of $\pm 24^\circ$ is generated. The phase increases up to an attenuation range of 13 dB; for higher attenuation ranges, the phase decreases.

B. Varying the Drain–Source Voltage with Fixed Gate–Source Voltage (Amplifier B)

Fig. 4 shows the simulated phase and amplitude characteristic of the variable-gain amplifier when the drain voltage is varied and the gate–source voltage is fixed. Within a control voltage from 0 to 1.5 V and a corresponding amplitude control range of 20 dB, the phase decreases with decreasing gain and a phase deviation of $\pm 30^\circ$ is generated.

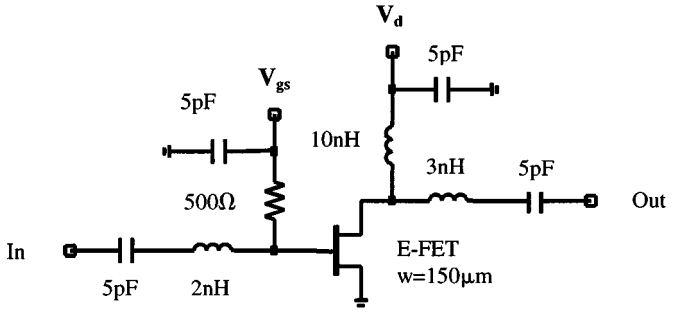

Fig. 2. Schematic of the variable-gain amplifier, the gain can be controlled by $V_{\rm gs}$ or V_d.

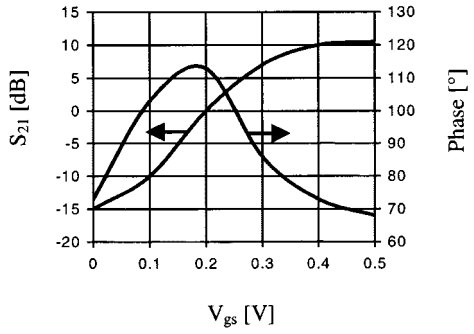

Fig. 3. Amplifier A: simulated phase and amplitude characteristic. $V_{\rm gs}$ is varied, $V_d = 1.5$ V, and $f = 5.2$ GHz.

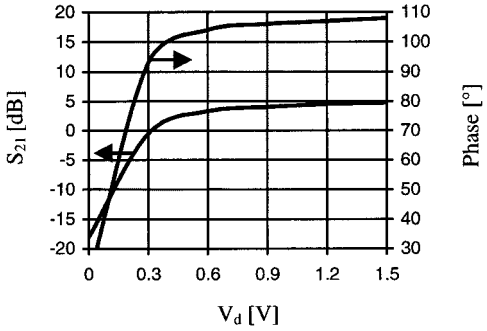

Fig. 4. Amplifier B: simulated phase and amplitude characteristic. V_d is varied, $V_{\rm gs} = 0.25$ V, and $f = 5.2$ GHz.

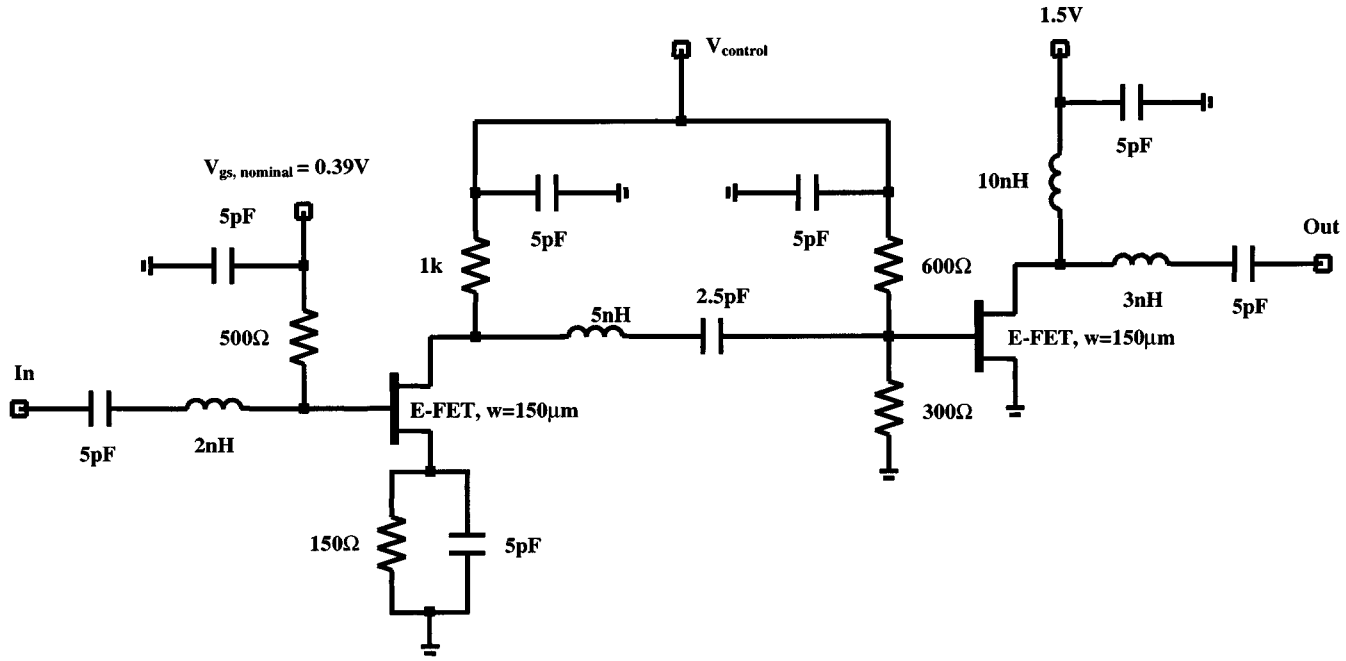

Fig. 5. Schematic of the proposed amplifier: amplifier A (right-hand side) and amplifier B (left-hand side) are cascaded, the gate bias of amplifier B is stabilized using the circuit shown in Fig. 6.

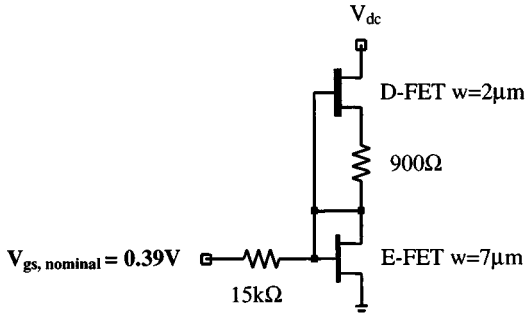

Fig. 6. Bias circuit to decrease the influence of threshold voltage variations.

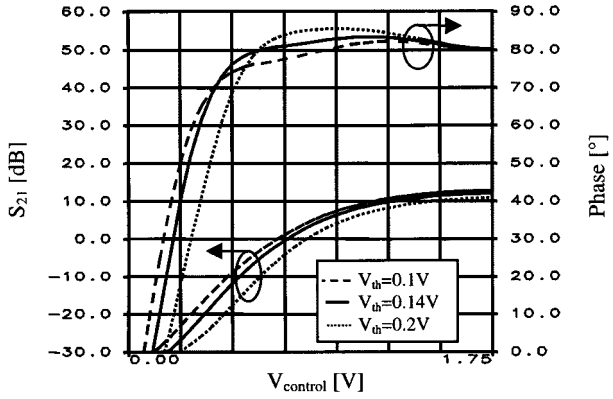

Fig. 7. Simulated phase and amplitude characteristic of the proposed amplifier (Fig. 5) for different threshold voltages ($V_{\rm th}$). $f = 5.2$ GHz.

C. Proposed Circuit to Suppress the Transmission Phase Error

The phase errors of amplifiers A and B would create unacceptable phase and amplitude errors in vector modulators when a nominal lookup table is applied, or would require a complex calibration procedure for compensation.

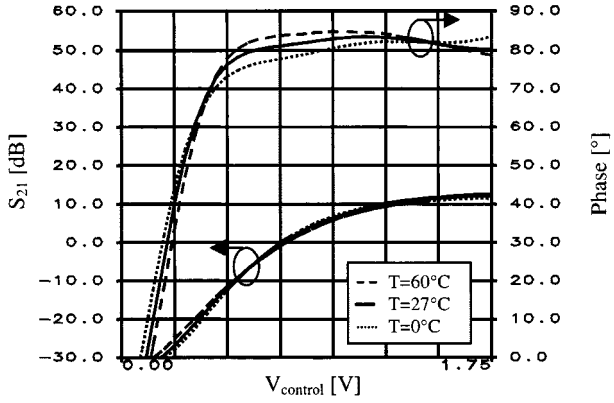

Fig. 8. Simulated phase and amplitude characteristic of the proposed amplifier (Fig. 5) for different temperatures (T). $f = 5.2$ GHz.

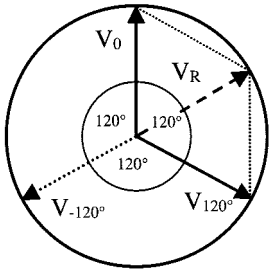

Fig. 9. Vector addition: every phase with amplitude V_R can be obtained by weighting two of the vectors V_0, V_{120°, and V_{-120°.

We propose the following principle to suppress the phase error of variable-gain MESFET amplifiers. A suitable combination of the phase characteristics of amplifiers A and B enables a

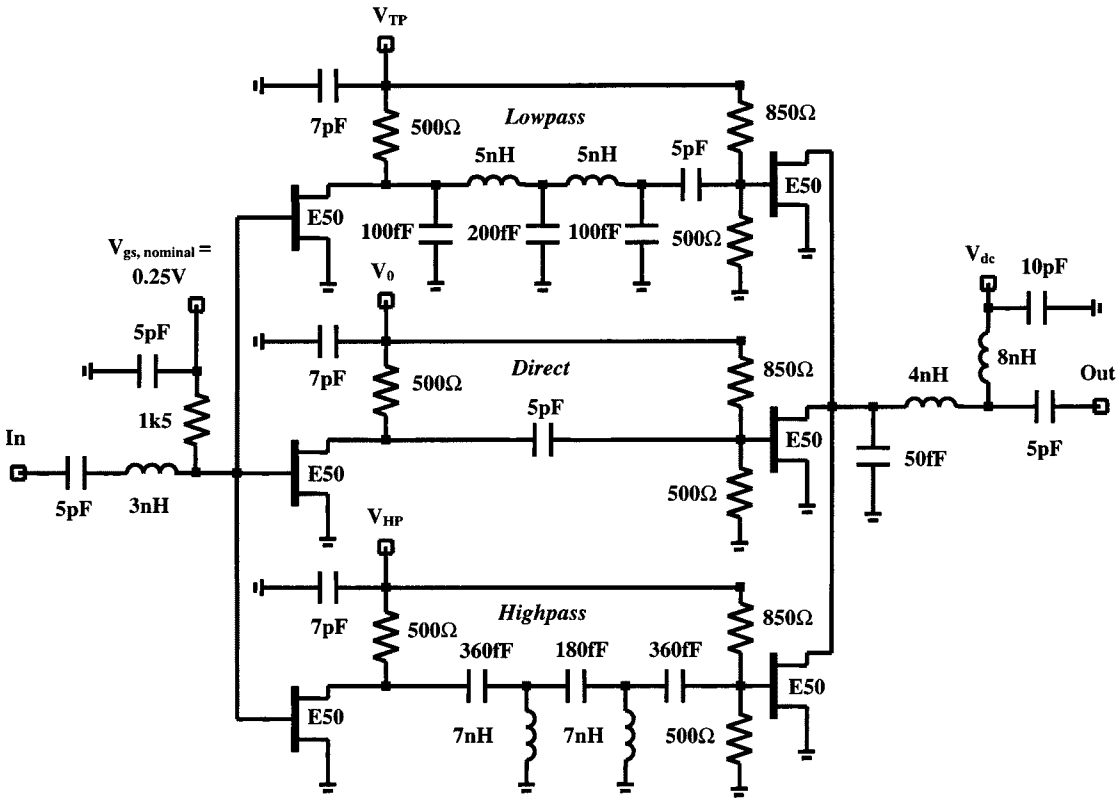

Fig. 10. Simplified circuit schematic of the vector modulator, the gate bias of the power divider FETs is generated using a bias circuit similar to that shown in Fig. 6.

compensation of the phase errors. We utilize the fact that, up to a limited, but sufficient attenuation range, the phases of amplifiers A and B change in the opposite direction.

Fig. 5 shows the proposed circuit, which is a cascade circuit of amplifiers A and B. V_{control} connects the drain–source voltage of amplifier B with the gate–source voltage of amplifier A. A voltage divider is applied to set the optimum gate–source voltage of amplifier A. The dc operating point of amplifier B can be influenced by a drain bias resistor. The transition point from the saturation region to the resistive region can be adjusted with this resistor to influence the corresponding phase characteristic. Our simulations showed that phase and amplitude characteristics are highly influenced by the variation of the threshold voltage. A gate-bias circuit (Fig. 6) and a dc feedback in the source are applied to amplifier B to decrease the influence of threshold voltage variations.

The simulated phase and amplitude characteristic of the proposed amplifier is shown in Fig. 7 for threshold voltages of 0.1, 0.14, and 0.2 V. Within a control voltage from 0.6 to 1.75 V and a corresponding gain control range of 20 dB, the phase variation can be reduced to $\pm 3^{\circ}$. Fig. 8 shows the influence of temperature changes within ± 30 °C. The circuit is relatively insensitive to temperature variations. We also investigated the variation of other MESFET parameters within process tolerances. Simulations show that their impact to the functionality of the proposed principle is negligibly small.

The proposed principle is successfully applied to the designed vector modulator described in Section III.

III. Vector Modulator

A. Requirements

The vector modulator has been designed for minimum dc power consumption and chip size. A gain of about 0 dB is desired. The HIPERLAN receiver requires an 1-dB input compression point ($P_{1\,\mathrm{dBcomp.,\,input}}$) of -20 dBm. If we assume that a variable-gain low-noise amplifier with a maximum gain of about 10 dB is located in front of the vector modulator, the requirement for the 1-dB input compression point of the vector modulator is approximately -10 dBm. A previous work [8] showed that phase and gain resolutions of approximately $\pm 5^{\circ}$ and ± 0.5 dB are reasonable demands.

B. Design

Usually, four signal paths with phase offsets of 90° are used for vector modulators. To minimize chip size and control complexity, we use three signal paths with phase offsets of 120° [5]. Every desired phase within the 360° phase control range can be obtained by weighting the amplitudes of two of the three phase paths. This is illustrated in Fig. 9 for the phase control sector from 0° to 120°. Adequate characteristics are obtained for the phase control sectors from 0° to 120° and -120° to 120°, respectively.

The simplified schematic of the designed vector modulator is shown in Fig. 10. The circuit was fabricated with the Triquint TQTRx foundry process, which provides inductances with a quality factor of about 20. Low power-consuming enhancement

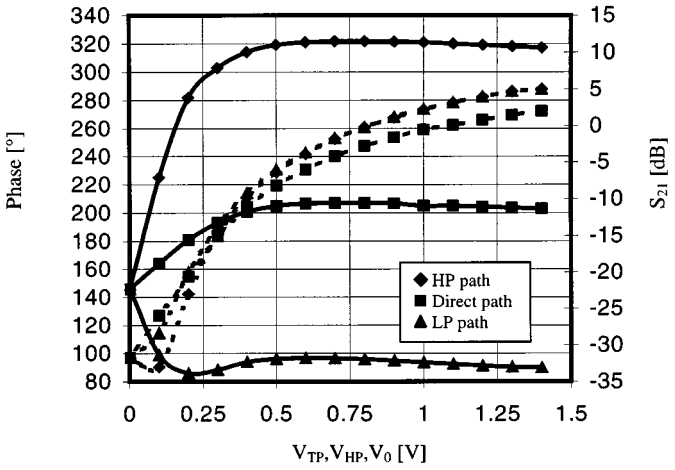

Fig. 11. Measured phase (solid line) and amplitude (dotted line) characteristic of each of the three paths, when the other paths are switched off.

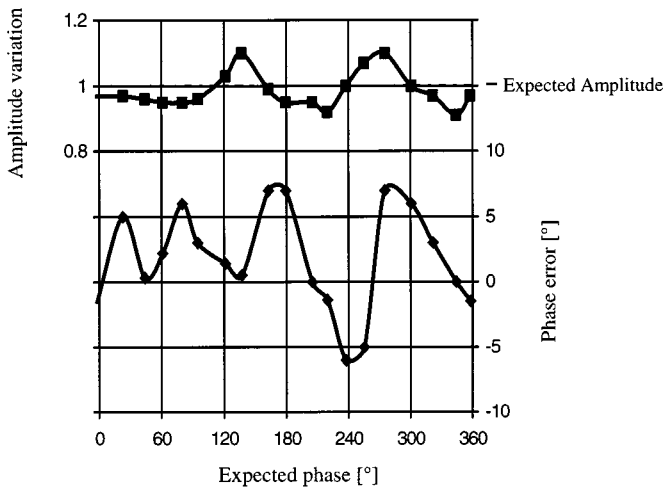

Fig. 13. Normalized amplitude variation and phase error of the vector modulator using the proposed calibration.

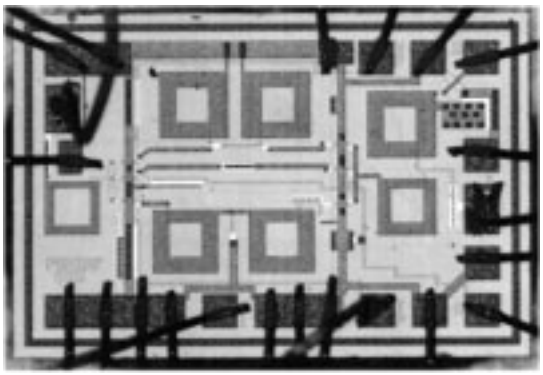

Fig. 12. Photograph of the vector modulator MMIC (chip size $\sim$0.9 mm $\times$ 1.4 mm).

FETs with gatewidths of 50 μm and gate lengths of 0.6 μm are used to divide, respectively, to combine the signal paths. The 120° phase offsets of the signal paths are generated by HP and LP structures with an impedance of approximately 200 Ω. This high interstage impedance has two significant advantages. First, large-signal simulations predict a better intermodulation behavior for the low current operation of the power divider FETs. Second, no interstage *LC* matching is necessary. Note that the bias resistors with relatively small values improve the matching. The amplitudes of the signal paths can be controlled by the analog voltages $V_{\rm HP}$, V_0 and $V_{\rm TP}$ within a voltage range from 0 to 1.4 V. The power divider/combiner FETs are used as variable-gain amplifiers similar, as explained in Section II-C, to suppress the transmission phase error of the paths. Input and output are *LC* matched to 50 Ω. Fig. 11 shows the measured phase and amplitude characteristics of each of the three signal paths, when the other two paths are switched off. Within amplitude ranges of 15 dB, the maximum phase errors are only $\pm 4^\circ$.

A photograph of the vector modulator chip is shown in Fig. 12. The chip was bonded on a test substrate. The required chip area is only 1.3 mm^2.

C. Calibration

To reach a high yield within process variations and temperature changes, a suitable calibration is required. A calibration signal can be fed as shown in Fig. 1. We assume that the baseband signal processor can be used for the calibration algorithms. The calibration of the vector modulator can be repeated in defined time intervals to adapt to temperature variations of the environment.

With the assumption that the phase variations of the variable-gain amplifiers are negligible, we propose the following calibration procedure.

1) Measurement of the transmission amplitude of each of the three vector paths versus the corresponding control voltage, which is swept from 0 to $V_{\rm max}$ (0–1.4 V), while the other two vector paths are switched off (control voltages are 0 V).
2) Measurement of the transmission phase of each of the three vector paths at one base control voltage (0.9 V), while the other two vector paths are switched off (control voltages are 0 V).
3) Calculation of the required control voltages for the desired phases and fixed amplitude by vector addition using the data obtained from 1) and 2).

D. Results

A lookup table was created by measurements to verify the proposed calibration procedure. A fixed amplitude was set $(S_{21} = 0.6\,\text{dB})$. The obtained values were compared with the values given by the proposed calibration procedure. Fig. 13 shows the amplitude variation (normalized to the expected amplitude) and the phase errors versus the expected phase. The maximum phase errors are within $\pm 7^\circ$. The amplitude variation is smaller than ± 0.4 dB. Note that the corresponding maximum gain error is ± 0.8 dB.

The deviations obtained using the calibration procedure are, in particular, caused by the nonideal power divider/combiner function of the MESFETs and the nonconstant phases of the paths.

TABLE I
MEASURED PERFORMANCES OF THE VECTOR MODULATOR AT 5.2 GHz USING THE PROPOSED CALIBRATION

V_{supply}	I_{supply}	$P_{1dB\ comp.,\ input}$	Gain	Chip area	Gain resolution	Phase resolution
[1.4V.. 5V]	[3.5mA.. 7mA]	>-9dBm	0.6dB	~1.3mm^2	±0.8dB	±7°

Table I summarizes the measured performance of the vector modulator. The design goals are fulfilled with a power consumption of less then 10 mW using a 1.4-V supply. The 1-dB input compression point is higher than −9 dBm. The noise figure is better than 7 dB and the gain is 0.6 dB.

IV. CONCLUSION

This paper has demonstrated the design and the results of a vector-modulator-based phase-shifter MMIC. The chip is very small, operates with low voltage supplies, and is designed for a HIPERLAN smart antenna receiver. The proposed vector modulator contributes considerably to the reduction of power consumption, chip size, and costs. A new principle is proposed to improve the transmission phase characteristics of variable-gain amplifiers, which are required in vector modulators. This enables a simple calibration procedure to reach high yields regarding foundry process tolerances and temperature changes of the environment.

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Urs Lott (S'79–M'83) was born in Zürich, Switzerland, in 1959. He received the Dipl. Ing. degree in electrical engineering and the Ph.D. degree from the Swiss Federal Institute of Technology (ETH) Zürich, Zürich, Switzerland, in 1983 and 1990, respectively.

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